S7880 Touch Controller Datasheet

PN: 505-000683-01 Rev. 1

Introduction

The Synaptics® S7880 touch controller is a high performance TouchPad controller with up to 43 sensing channels for use in touchscreens up to 7 inches in diagonal with a 16:10 aspect ratio and a sensor pitch of 6 mm. The maximum number of nodes is 442 (for example, a 26 RX x 17 TX configuration). The S7880 is recommended for use in automotive applications.

General description

The S7880 supports self-capacitance, mutual-capacitance, and hybrid sensing with up to 10-finger detection. Fast report rates (up to 100 Hz) and flexible sensing frequency from 50 to 500 kHz are also supported.

The S7880 provides high performance hardware filtering for noise mitigation, moisture detection, and severe common mode noise rejection. The device also offers high performance charge pump, patented Synaptics SignalClarity™ driving schemes, and advanced firmware algorithms.

Features and benefits

- ISO-TS16949 compliant
- AEC-Q100 qualification to Automotive Grade 2 (–40ºC to 105ºC) (completion Q1/2017)
- Production Part Approval Process (PPAP) documentation (completion Q1/2017)
- 64TQFP package (10 mm x 10 mm x 1.0 mm)
- Glove detection
- Moisture mitigation
- Thick lens support (4 mm at a dielectric constant of 8)
- Curved lens designs with maximum thickness same as thick lens support with any minimum thickness
- Power modes:
  - Touch active
  - Normal operation
  - Sensor sleep
- Serial interfaces:
  - I^2C (100/400 kHz)
  - SPI slave
- Power supply schemes:
  - 2.7V to 3.6V supply voltage
  - Internal charge pump for increased TX voltage up to 6.6V
- Best-in-class capacitance sensing:
  - Up to 10-finger detection and simultaneous tracking
  - Optimum SNR performance: on-chip charge pump with SignalClarity
- In-system reprogrammability (reflash) support
- Internal power-on reset detector
- Hardware filtering for noise mitigation
- Supports configurable frequency shifting
- Supports advanced sensor/display architecture including:
  - Touch controller on sensor FPC tail
  - Touch controller on main board
- On-Cell sensor designs
- Built-in self test (BIST) feature
- Self-calibrating — no host side calibration needed
- Fully compatible with Synaptics Design Studio™ 5 tool chain for production-ready touch sensing development

Contents

Architecture

The S7880 is a fully self-contained, ready-to-use, capacitance-sensing system on a chip (SoC). Synaptics proprietary microcontroller and firmware handle all calibration, capacitance-sensing, computation of finger position, and gesture reporting.

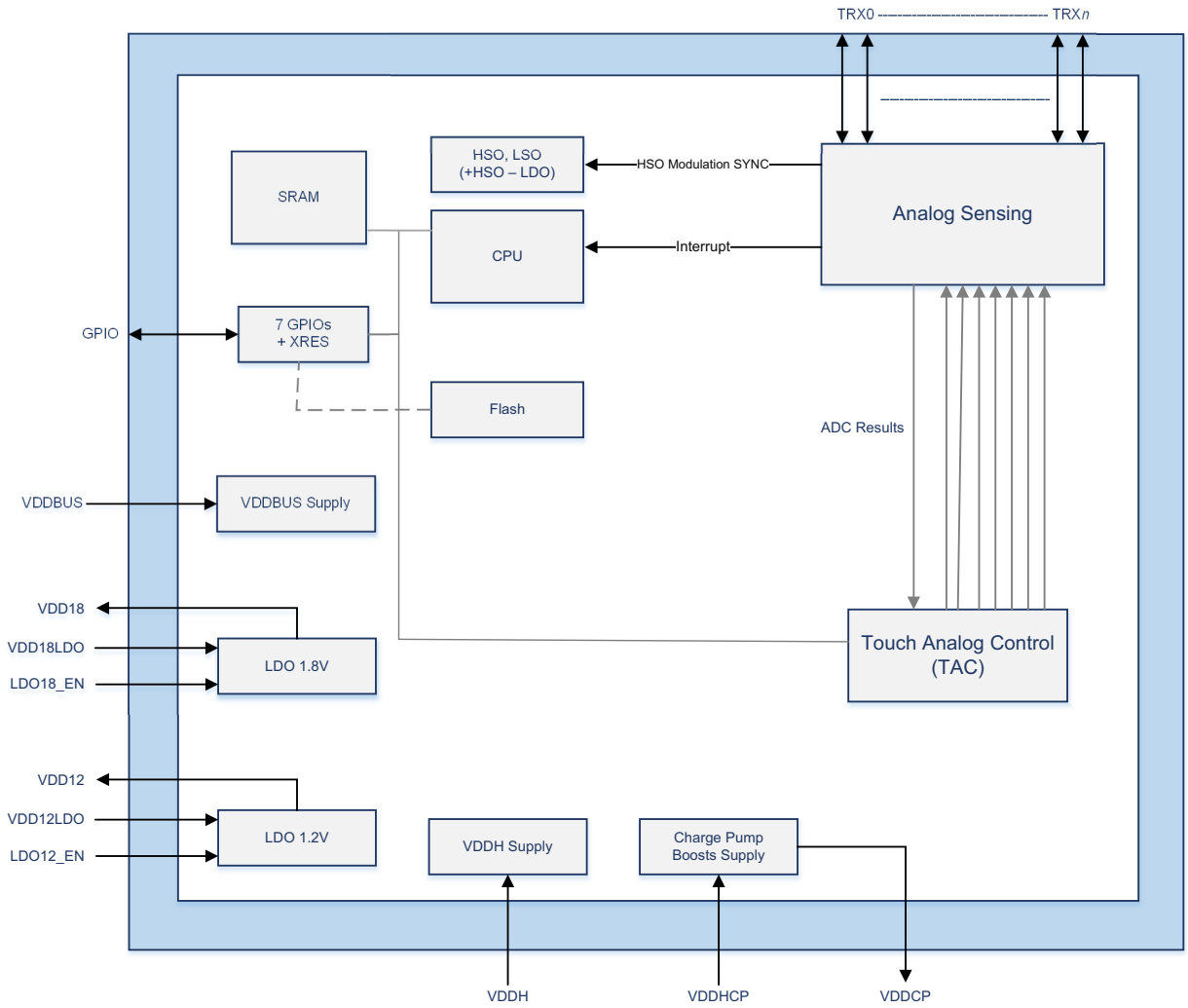

Figure 1. S7880 block diagram

Pin assignments

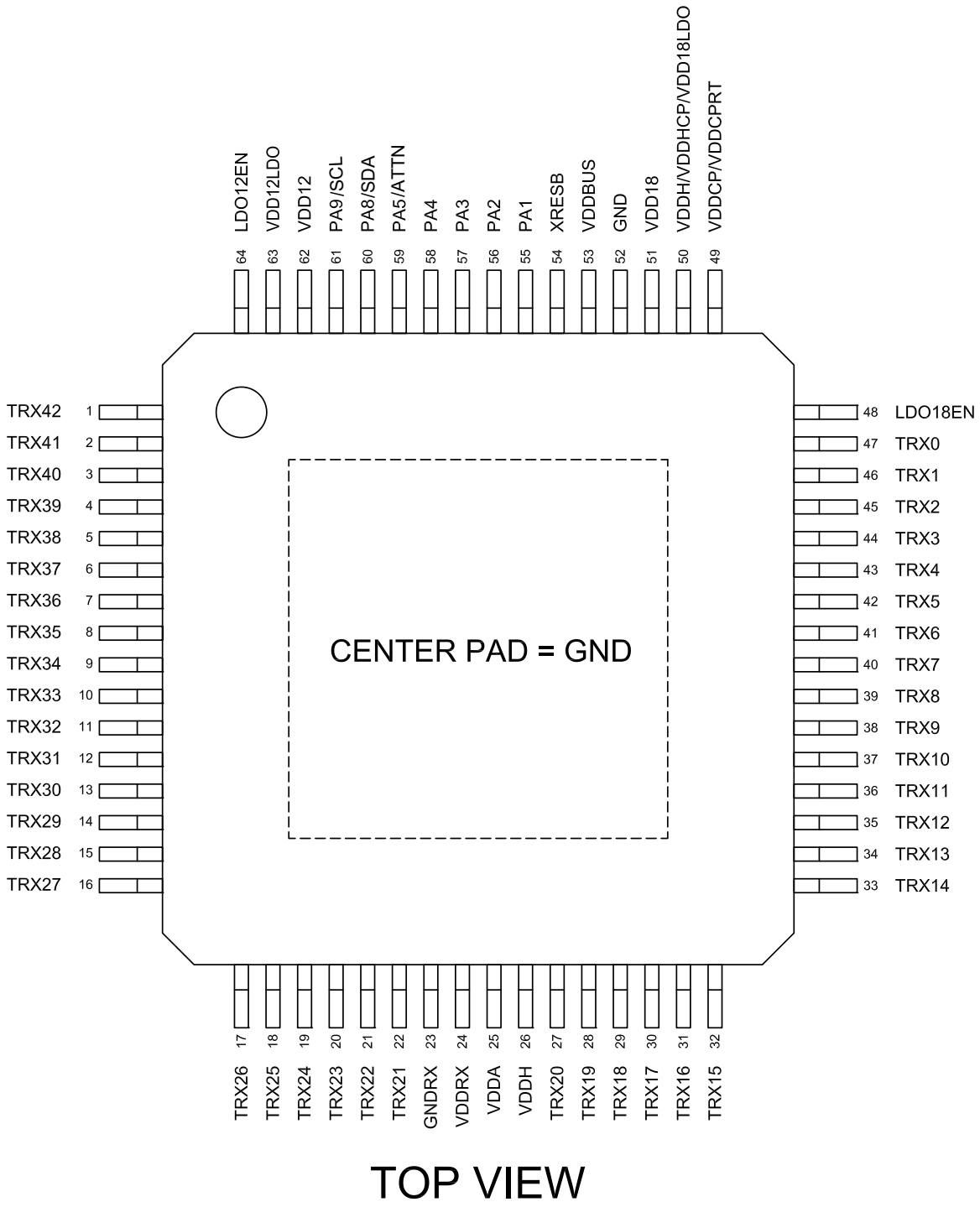

Figure 2. S7880 pin assignments (top view)

Pin definitions

Table 1. S7880 pin definitions

Pin Location	Signal	Type	Description
1	TRX42	I/O	Transmitter or receiver electrode, E Bank, configurable in bank grouping.
2	TRX41	I/O	Transmitter or receiver electrode, D Bank, configurable in bank grouping.
3	TRX40	I/O	Transmitter or receiver electrode, D Bank, configurable in bank grouping.
4	TRX39	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
5	TRX38	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
6	TRX37	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
7	TRX36	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
8	TRX35	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
9	TRX34	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
10	TRX33	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
11	TRX32	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
12	TRX31	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
13	TRX30	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
14	TRX29	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
15	TRX28	I/O	Transmitter or receiver electrode, C Bank, configurable in bank grouping.
16	TRX27	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
17	TRX26	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
18	TRX25	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
19	TRX24	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
20	TRX23	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
21	TRX22	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
22	TRX21	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
23	GNDRX	I/O	Filtered analog ground.
24	VDDRX	Filter Pin	Filtered from VDDH analog power.
25	VDDA	Filter Pin	Filtered from VDDH charge integrator's power.
26	VDDH	Power	3V analog power input.
27	TRX20	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
28	TRX19	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
29	TRX18	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
30	TRX17	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.

Table 1. S7880 pin definitions (Continued)

Pin Location	Signal	Type	Description
31	TRX16	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
32	TRX15	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
33	TRX14	I/O	Transmitter or receiver electrode, B Bank, configurable in bank grouping.
34	TRX13	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
35	TRX12	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
36	TRX11	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
37	TRX10	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
38	TRX9	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
39	TRX8	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
40	TRX7	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
41	TRX6	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
42	TRX5	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
43	TRX4	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
44	TRX3	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
45	TRX2	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
46	TRX1	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
47	TRX0	I/O	Transmitter or receiver electrode, A Bank, configurable in bank grouping.
48	LDO18EN	I	Connect to VDDH.
49	VDDCP/ VDDCPRT	Power	Power input to the charge pump bypass switch or output of charge pump.
50	VDDH	Power	3V analog power input.
51	VDD18	Power	Output of internal 1.8V LDO.
52	GND	Ground	Package analog ground
53	VDDBUS	Power	Connect to VDDH. Power supply for all GPIO pins.
54	XRESB	I	Dedicated active low reset pin; has internal pull-up to VDDBUS.
55	PA1	GPIO	Spare GPIO.
56	PA2	GPIO	Spare GPIO.
57	PA3	GPIO	Spare GPIO.
58	PA4	GPIO	Spare GPIO.
59	PA5/ATTN	GPIO	I^2C ATTN interrupt.
60	PA8/SDA	GPIO	I^2C data (SDA); true open drain I/O.

Table 1. S7880 pin definitions (Continued)

Pin Location	Signal	Type	Description
61	PA9/SCL	GPIO	I^2C clock (SCL); true open drain I/O.
62	VDD12	Power	Output of internal 1.2V LDO.
63	VDD12LDO	Power	Connect to VDD18 (pin 51).
64	LDO12EN	I	Connect to VDD18 (pin 51).

Note: Back pad must be connected to GND.

Transmitter and receiver configurations

Table 2. S7880 transmitter and receiver bank options

Bank	TRX	Number of TRX
A0	TRX0 to TRX11	12
A1	TRX12 to TRX13	2
B0	TRX14 to TRX25	12
B1	TRX26 to TRX27	2
C	TRX28 to TRX39	12
D	TRX40 to TRX41	2
E	TRX42	1

Configuration pin options

Table 3. S7880 axis setting options

Bank	Axis Setting	
	0x33	**0x0C**
A0	12R	12T
A1	2R	2T
B0	12T	12R
B1	2T	2R
C	12R	12T
D	2R	2T
E	1T	1T
Total	28R; 15T	14R; 29T

Sample schematic

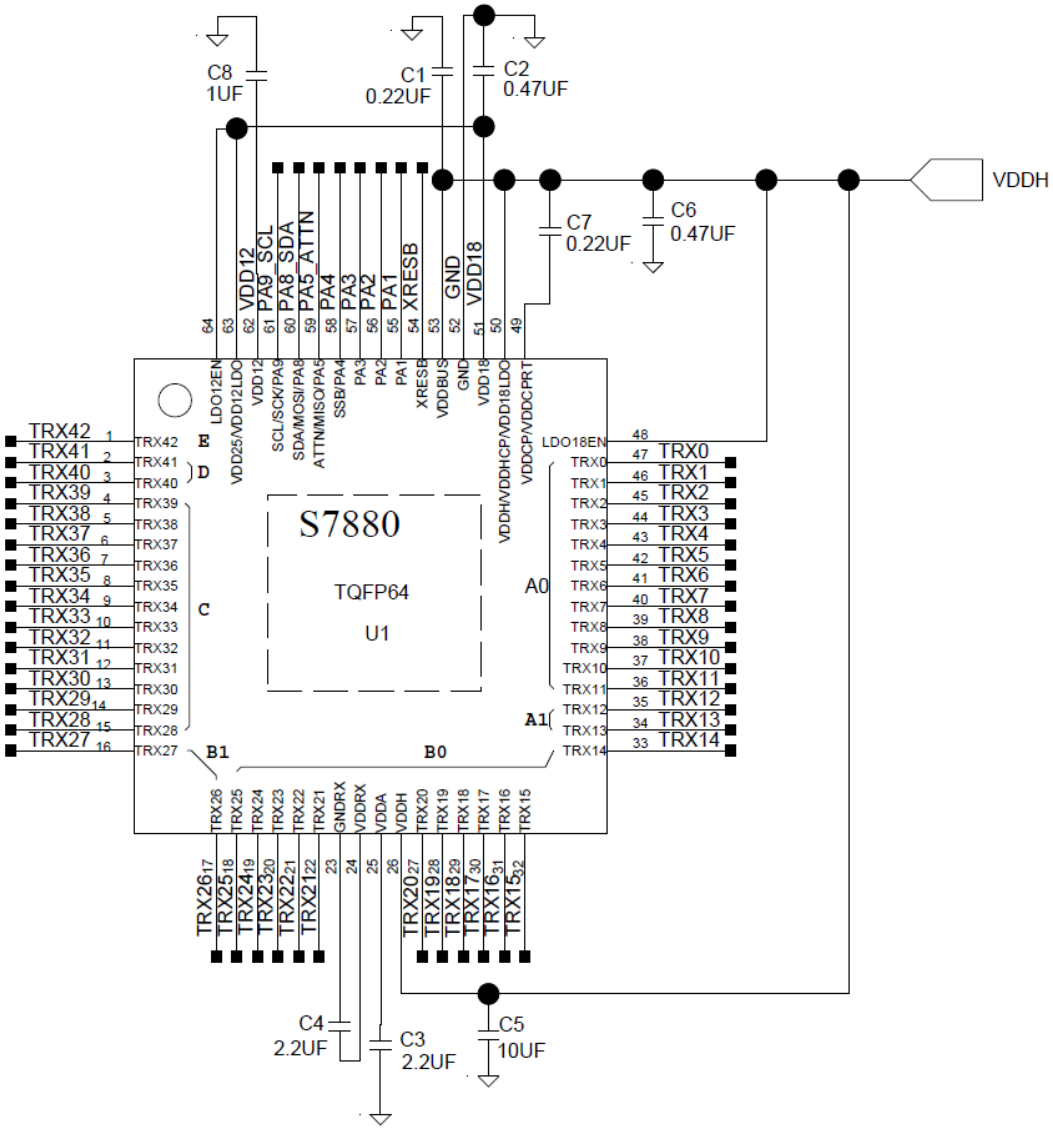

Figure 3. S7880 schematic

Note: Place capacitors as close to power supply pins as possible.

Note: Both VDDH pins are externally connected.

Power supply configuration

The S7880 is designed for a single external power supply rail. Table 4 provides the possible configuration. For details on sensor/FPCA design and routing guidelines, refer to the *ClearPad Sensor Design Guidelines* (PN: 511-000384-01).

Table 4. S7880 power supply configuration

VDD12	VDD18	VDDH	VDDBUS	LDO12EN	LDO18EN	Description
Internal	Internal	External	Connect to VDDH	Connect to VDD18	Connect to VDDH	External VDDBUS and VDDH Internal 1.8V, 1.2V

Note: The VDDBUS shares an external power supply with VDDH. VDDBUS must follow the VDDH power specification in Table 6.

Host interface

The S7880 is available with an I²C host interface. The host communicates with the S7880 by reading and writing 8-bit data registers. Full details of Synaptics interface protocols can be found in the *Synaptics RMI4 Specification* (PN: 511-000405-01).

Attention signal

In addition to standard I²C signals, the S7880 provides an *attention* output (ATTN) that is asserted to indicate that new data is available for reading by the host. The ATTN signal is intended to be used as an interrupt source to a host processor. ATTN functionality is added by user interface firmware so pin allocation, polarity and drive options (open-drain or push-pull) are defined at the time of firmware build. Operation of the ATTN signal is shown in Figure 4.

I²C interfacing

Connection

Figure 5 shows an example of host connection using the S7880 I²C interface. The values of the pull-up resistors should be chosen to ensure that the rise times of the SDA and SCL signals are within the limits set by the I²C specification. This depends on what other slave devices, if any, are on the I²C bus but typically would fall within the range of 2.2 kΩ –10 kΩ.

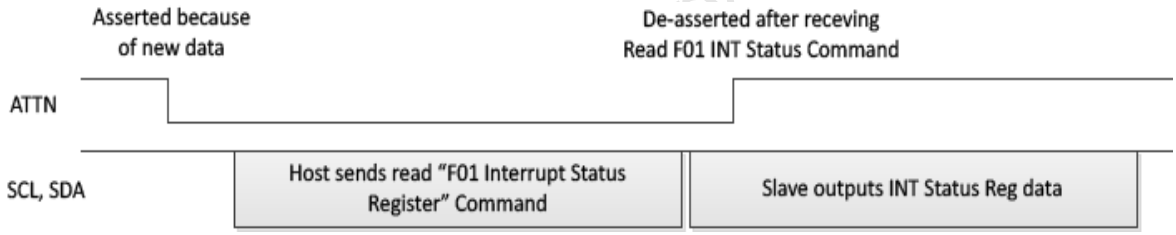

Figure 4. Attention line behavior (I²C interface shown)

Note: The attention line is also de-asserted when the host disables interrupts.

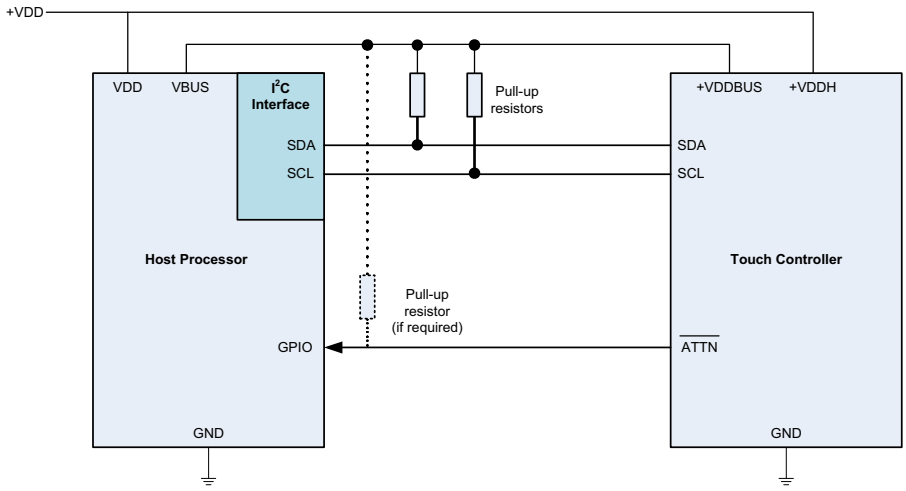

Figure 5. Typical connection of the touch controller to the host

Clock stretching

Special attention should be paid to clock stretching when interfacing with a Synaptics touch controller over I^2C. The host processor must support clock stretching. The first byte of a transaction contains the slave address and read/write bit. At the end of the first byte, the touch controller holds SCL low (clock stretches) and checks that the slave address matches its own. If the slave address does not match, the S7880 will not stretch the clock on subsequent byte transmissions until it detects the next start condition. If the slave address does match, the touch controller acknowledges and may stretch the clock after some or all of the subsequent bytes within the same transaction (Figure 6).

Note: Typical clock stretch time (Tcstr) is less than 25 ms.

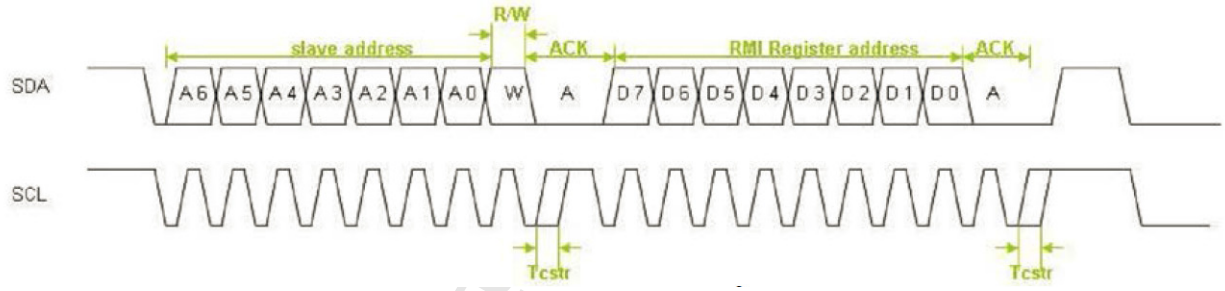

Figure 6. Clock stretching with an I^2C transaction

In-system reprogrammability

The S7880 includes firmware in order to support finger tracking and position reporting. This firmware is stored in non-volatile (flash) memory on-chip and may be updated at any time over the host interface. This capability allows freedom and flexibility when operating with Synaptics devices; simply choose the firmware image that is applicable to your design. Figure 7 illustrates the firmware storage methodology.

Note: Reference code is available from Synaptics that implements the steps for reprogramming the configuration and user interface firmware space.

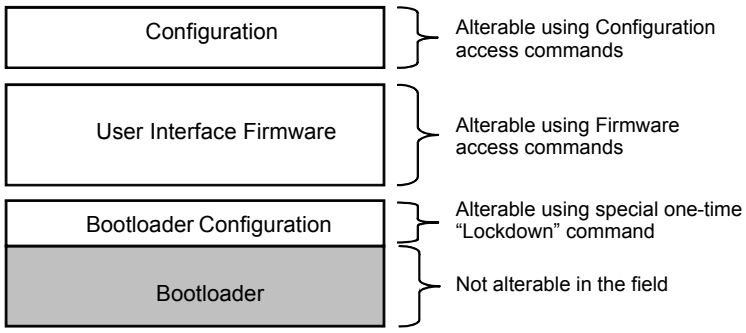

Figure 7. Firmware structure

Configuration

The configuration space stores the default values of the device's control registers. The bootloader provides a mechanism to erase and reprogram this space. Because an existing configuration may not be valid for a new firmware revision, any update to the user interface firmware should be followed by an update of the configuration space.

User interface firmware

The user interface firmware space contains the firmware that implements the primary function of the device.

User interface firmware images are provided by Synaptics in an encrypted form to ensure they can only be executed on an appropriate device. It is not possible to erase the user interface firmware space without also erasing the configuration space.

Bootloader configuration

This can be set by a one-time lockdown process when adding user interface firmware for the first time. This permits the same S7880 parts to be deployed in different hosts systems where required bootloader configuration may be different for each.

Bootloader

This is pre-programmed and cannot be changed. The bootloader:

- checks the integrity of the user interface firmware space
- provides the ability to re-flash a new user interface or configuration area.

Electrical specifications

Absolute maximum ratings

Table 5. S7880 absolute maximum ratings

Parameter	Minimum	Maximum	Unit
Voltage on any GPIO pin	–0.3	3.6	V
VDDBUS	–0.3	3.6	V
VDD12	–0.3	1.32	V
VDD18	–0.3	1.98	V
VDDH/VDDHCP	–0.3	3.6	V
Input current at any pin	—	100	mA
Package input current	—	200	mA
Operating temperature	–40	105	°C
Storage temperature, unbiased	–55	125	°C
Lead soldering temperature (10 seconds)	—	260	°C

Note: When the input voltage at any pin exceeds the associated power supply, the current at that pin should be limited to 100 mA. The 200 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 100 mA to two pins. The maximum time this condition can be applied is approximately 10 seconds.

Note: Stresses beyond those listed in Table 5 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: The absolute maximum junction temperature (Tjmax) for this device is 150 °C.

Note: VDDBUS should not be higher than VDDH.

Device level specifications

Table 6. S7880 DC characteristics

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
Analog supply input 1	VDDH	—	2.7	3.3	3.6	V
Analog filter pin 1	VDDRX	Internally filtered power	2.6	—	3.6	V
Analog filter pin 2	VDDA	Internally filtered power	2.6	—	3.6	V
Digital core supply	VDD12	—	1.14	1.2	1.32	V
Analog supply input 2	VDD18	—	1.71	1.8	1.98	V
Internal 1.2V LDO supply input	VDD12LDO	Connect to VDD18	1.62	1.8	1.98	V
Internal 1.8 LDO supply input	VDD18LDO	Connect to VDDH	2.7	—	3.6	V
GPIO power supply	VDDBUS	Shared with VDDH	VDDH	—	VDDH	V
Analog supply input for charge pump and LDO	VDDHCP	Connect to VDDH	2.7	3.3	3.6	V
Charge pump output	VDDCP	Typically 2x VDDH	5.4	—	7.2	V
Power supply ripple	—	—	—	—	100	mV (peak-to-peak)

Table 7. S7880 capacitance characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Mutual capacitance	C_T	Mutual capacitance per node	—	1.5	—	pF
Mutual capacitance resolution	C_{TR}	—	—	2.2	—	fF
Column self capacitance	C_B	Self capacitance per channel	—	60	—	pF
Row self capacitance	C_B	Self capacitance per channel	—	60	—	pF
Self capacitance resolution	C_{BR}	—	—	14	—	fF

Note: The values listed are typical capacitance values for sensors.

Reliability characteristics

Table 8. S7880 reliability characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Reference Test Method
$FLASH_{DR}$	Flash data retention	10	—	Years	Accelerated test
$FLASH_{ENPB}$	Flash write endurance	1,000	—	Erase/Write Cycles	—
V_{ZAPHBM}(1)	ESD susceptibility HBM	—	± 2	kV	Class 2 (AEC Q100-002/JEDEC JS-001)
V_{ZAPCDM}(1)	ESD susceptibility CDM	—	± 750 corner pins ± 500 rest of pins	V	Class C4B (AEC Q100-011)

Note 1: This parameter is tested initially during characterization and after a design or process change that affects the parameter.

GPIO characteristics

Push-pull GPIO characteristics

Table 9. S7880 push-pull GPIO characteristics

Mode	Function	Condition	Input Low Level Voltage (V_{IL}) Maximum (V)	Input High Level Voltage (V_{IH}) Minimum (V)	Input Hysteresis (V_{HYS}) Typical (mV)	Input Capacitance (C_{IN}) Maximum (pF)	Output Voltage Low (V_{OL}) Maximum (V)	Output Voltage High (V_{OH}) Minimum (V)
0	I^2C standard or fast-mode	3.6V ≥ VDDBUS > 2.7V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	NA
1	I^2C standard or fast-mode	2.7V ≥ VDDBUS > 1.98V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	NA
2	I^2C standard or fast-mode	1.98V ≥ VDDBUS > 1.65V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.2 x VDDBUS	NA
3	GPIO	3.6V ≥ VDDBUS > 1.65V @ 1 MHz IOL = IOH = 20 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
6	SPI	3.6V ≥ VDDBUS > 1.65V @ 10 MHz maximum IOL = IOH = 10 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
6	GPIO	3.6V ≥ VDDBUS > 1.65V IOL = IOH = 10 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
7	Test	3.6V >= VDDBUS > 2.7V IOL = IOH = 30 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4

Open drain GPIO characteristics

Table 10. S7880 open drain GPIO characteristics

Mode	Function	Condition	Input Low Level Voltage (V_{IL}) Maximum (V)	Input High Level Voltage (V_{IH}) Minimum (V)	Input Hysteresis (V_{HYS}) Typical (mV)	Input Capacitance (C_{IN}) Maximum (pF)	Output Voltage Low (V_{OL}) Maximum (V)
0	I^2C standard or fast-mode	3.6V ≥ VDDBUS > 2.7V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4
1	I^2C standard or fast-mode	2.7V ≥ VDDBUS > 1.98V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.4
2	I^2C standard or fast-mode	1.98V ≥ VDDBUS > 1.65V IOL = 3 mA	0.3 x VDDBUS	0.7 x VDDBUS	0.05 x VDDBUS	10	0.2 x VDDBUS

Power management

The overall power supply current is a function of the operating power supplies, sleep mode, and product configuration, which can vary significantly. Synaptics measures power supply current as an average current on the power supply pins.

Table 11. S7880 nominal power supply current

Operating Mode	VDDH Current (mA) at 3.0V	Total Power (mW)
Sensor Sleep	0.09	0.267
Normal Operation	0.97	2.91
Active (1 Finger)	12.65	37.2
Active (5 Fingers)	13.10	38.8
Active (10 Fingers)	13.63	40.4

Timing characteristics

I²C

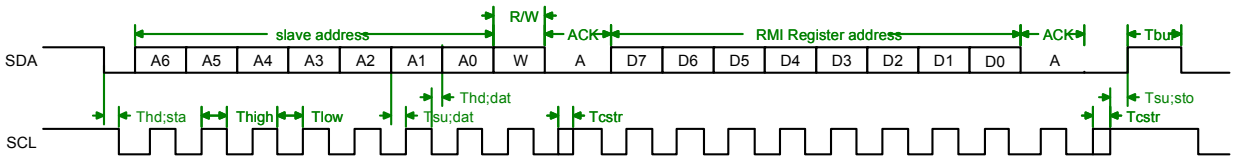

Figure 8. I²C timing

Table 12. I²C parameters

Parameter	Symbol	Standard-Mode			Fast-Mode			Unit
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
	f_{SCL}	—	—	100	—	—	400	kHz
Stretch time.	t_{CSTR}	—	25	25	—	25	25	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	—	—	0.6	—	—	µs
LOW period of the SCL clock.	t_{LOW}	4.7	—	—	1.3	—	—	µs
HIGH period of the SCL clock.	t_{HIGH}	4.0	—	—	0.6	—	—	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	—	—	0.6	—	—	µs
Data hold time.	$t_{HD;DAT}$	0	—	3.45	0	—	0.9	µs
Data out valid time.	$t_{VALID;DATO}$	—	—	3.45	—	—	0.9	µs
Data set-up time.	$t_{SU;DAT}$	250	—	—	100	—	—	ns
Rise time of both SDA and SCL signals.	t_r	—	—	1000	$20 + 0.1C_b$	—	300	ns
Fall time of both SDA and SCL signals.	t_f	—	—	300	$20 + 0.1C_b$	—	300	ns
Set-up time for STOP condition.	$t_{SU:STO}$	4.0	—	—	0.6	—	—	µs
Bus free time between a STOP and START condition.	t_{BUF}	4.7	—	—	1.3	—	—	µs
Capacitive load for each bus line.	C_b	—	—	400	—	—	400	pF

Power-on sequence and initialization

VDDBUS supplies the communication I/O and GPIOs. VDDH supplies analog power. VDD18 and VDD12 supply the digital IC core power. The S7880 touch controller “Power OK” circuitry monitors the VDD18, VDD12, and VDDBUS supply inputs. In order for the POR cycle to commence, the power supplies must start at a lower voltage than the power OK falling threshold and rise monotonically and settle within their tolerances in 25 ms. All three power inputs must be valid before a power on reset condition begins (Figure 9).

The XRESB, external hardware reset input can also be used to force the chip into a reset condition, when the power supply cannot be shut off completely. The VDDBUS power input is provided so that the I^2C bus can remain functional while other power is removed from the touch controller. In this case the VDDBUS power will remain on and other devices that share the I^2C can continue to function. Pull-up resistors on the I^2C bus should be connected to VDDBUS. The SCL and SDA pins are true open-drain I/O pins and will not allow current leakage into the touch controller when the other power rails are switched off. VDDBUS also allows voltage translation with systems using from 1.8V to 3.3V logic.

VDDBUS, VDDH, VDD18, and VDD12 can be powered up in any order. The power state of VDDH is monitored by firmware. The touch controller ATTN interrupt output, typically GPIO PA5, has ESD protection devices that may allow current to leak from the pull-up resistor into the VDDBUS supply, when power is removed. For this reason it is important to connect pull-up resistors to the VDDBUS supply (and not other supplies). Another reason is that if VDDBUS and VDD18 are combined, the leakage current from the pull-up resistor may prevent the VDD18 from decaying fast after power is removed. And much time will be required for the voltage to decay low enough for the POR cycle to function normally.

When powering the S7880 touch controller up or down, system design should ensure that the voltages on the signal pins in the Absolute Maximum Ratings table are observed. Failure to follow this requirement may lead to unreliable operation of, or damage to, the device. Open-drain signals; for example, SCL/PA9 and SDA/PA8, are high-impedance at power-up and will transition high when the external pull-ups power (VDDBUS) is applied.

During the initialization phase ($T_{powerup}$), the touch controller reset and firmware initialization routines may take up to 45 ms. During this time, the ATTN signal will be de-asserted and no host commands will be recognized. After the touch controller is fully initialized, the ATTN pin will be asserted and host communication is enabled.

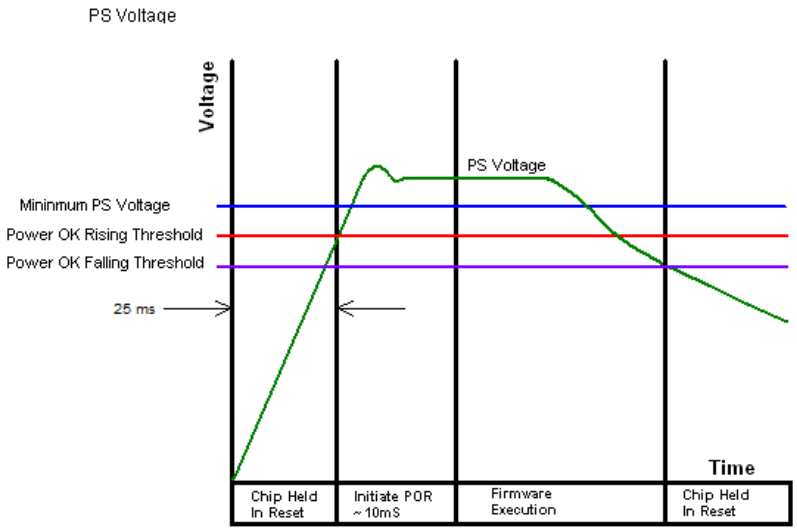

Figure 9. Power supply power-on sequence and start firmware execution

Power supply sequencing

The power supplies must start at below the power OK falling threshold and rise monotonically to their specified tolerance with 25 ms. Thereafter they must stay within the permitted tolerance. During power up when all power inputs are valid, I/O pin PA3 is driven high by the touch controller and will remain high until the hardware power on reset timer expires (minimum of 5 ms, maximum of 21 ms) at which time pin PA3 will pulse low. In systems where pin PA3 is used, the host should expect this power up pulse behavior. If this behavior is not tolerable, other GPIO pins should be used instead.

Important: It is strongly recommended to power-up the touch subsystem last in a device. Doing so allow s the touch controller to measure its baseline with other subsystems (such as an LCD) powered on, enabling optimized performance.

Table 13. Power OK characteristics

Power Supply	Power OK Rising Threshold	Power OK Falling Threshold	Power Supply Minimum Voltage	Unit
VDD12	1.08	1.02	1.14	V
VDD18	1.62	1.53	1.71	V
VDDBUS	1.62	1.53	1.71	V

Power-on interface timing

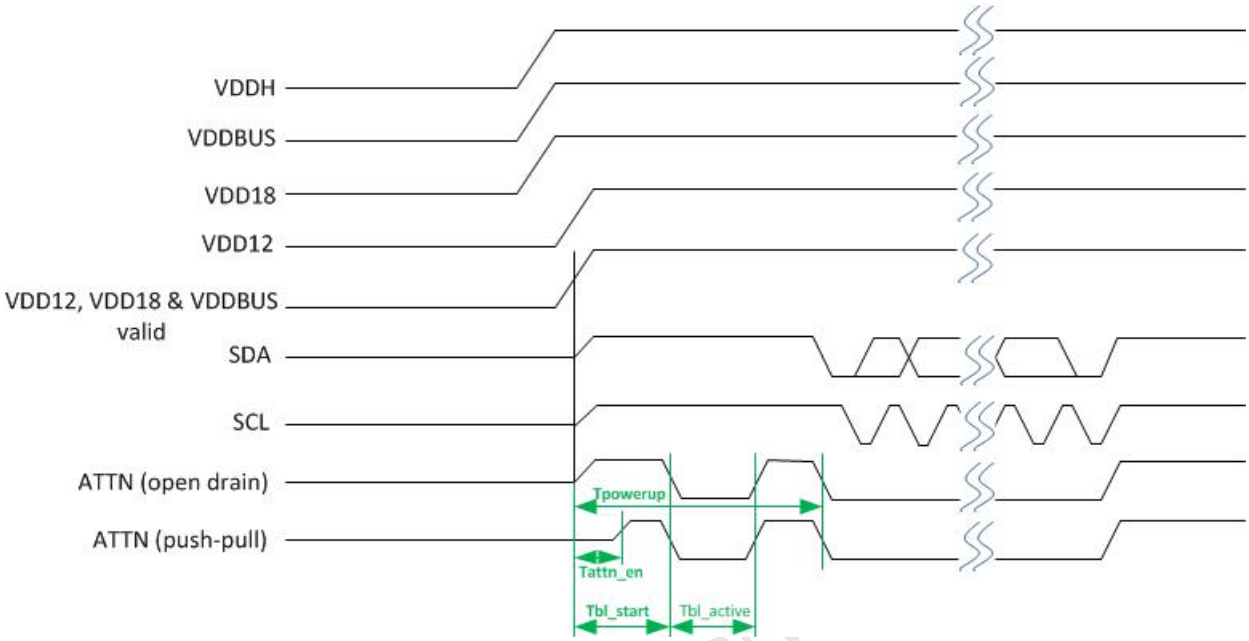

Figure 10. Power-on interface timing diagram

Table 14. Power-on sequence and external reset timing

Power Supply	Minimum	Maximum	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	—	45	ms
T_{bl_start} (bootloader start)	—	30	ms
T_{bl_active} (bootloader active)	—	15	ms
T_{reset} (XRESB pin)	100	—	ns

External reset timing

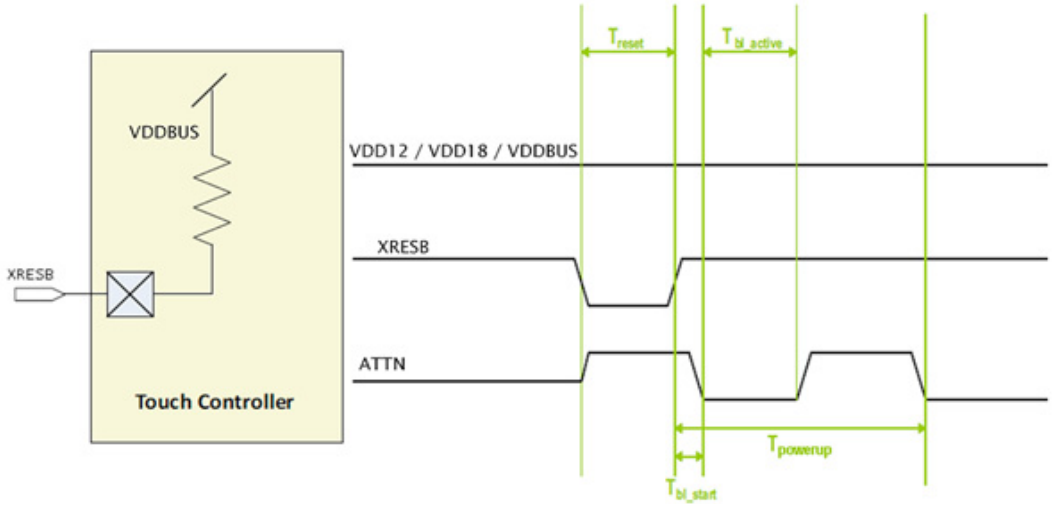

Figure 11. External reset timing diagram

Package and ordering information

Package drawing

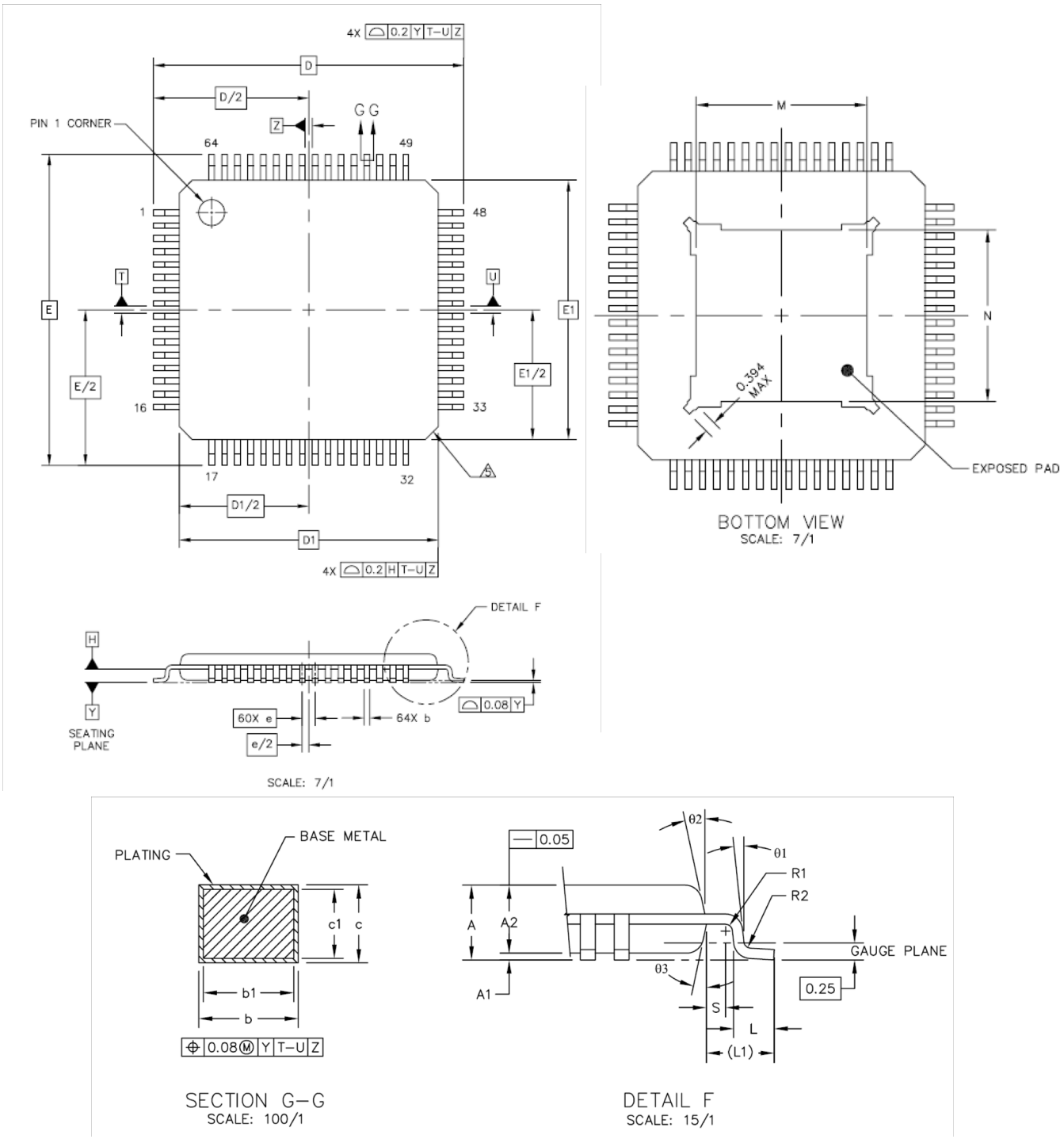

Figure 12. S7880 package drawing

Note: The exposed die attach pad should be connected to ground.

Dimensions

All measurements are in millimeters unless otherwise specified.

Table 15. S7880 dimensions

Aspect	Symbol	Common Dimensions		
		Minimum	Typical	Maximum
Total thickness	A	—	—	1.2
Stand off	A1	0.05	—	0.15
Mold thickness	A2	0.95	1	1.05
Lead width (plating)	b	0.17	0.22	0.27
Lead width	b1	0.17	0.2	0.23
L/F thickness (plating)	c	0.09	—	0.2
L/F thickness	c1	0.09	—	0.16
Body size	D	—	12 BSC	—
	D1	—	10 BSC	—
Lead pitch	e	—	0.5 BSC	—
Body Size	E	—	12 BSC	—
	E1	—	10 BSC	—
—	L	0.45	0.60	0.75
Footprint	L1	—	1 REF	
—	R1	0.08	—	
—	R2	0.08	—	0.2
—	S	0.2	—	
—	θ	0°	3.5°	7°
—	θ1	0°	—	—
—	θ2	11°	12°	13°
—	θ3	11°	12°	13°
EP Size	M	5.85	—	6.05
	N	5.85	—	6.05

Package marking

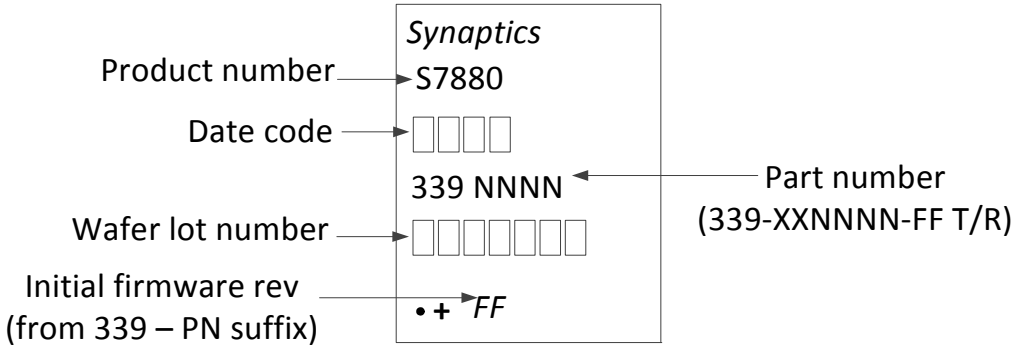

Figure 13. S7880 package marking

Ordering information

Refer to the *Touch Controller Ordering Guide* (PN: 511-000481-01) for ordering information.

Shipment packaging

The S7880 can be shipped either in trays or in tape-and-reel packaging.

For information about tape-and-reel packaging, see the *ASIC Tape-and-Reel Package Specification* (PN: 528-000187-01).

For tray packaging specifics, please contact Synaptics.

Environmental and regulatory compliance

This Synaptics product is built in compliance with the RoHS directive and the *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01). This Synaptics product is also Halogen-Free (HF) compliant.

Reference documents

- *ASIC Tape-and-Reel Package Specification* (PN: 528-000187-01)
- *ClearPad Sensor Design Guidelines* (PN: 511-000384-01)
- *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01)
- *Synaptics RMI4 Specification* (PN: 511-000405-01)
- *Touch Controller Ordering Guide* (PN: 511-000481-01)

Revision history

Table 16. Revision history

Revision	Description
1	Initial preliminary release.

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